Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 4. (Cancelled)

5. (Previously Presented) A transmission circuit to be used in a mobile communications system for transmitting transmission signals from a plurality of base stations with a matched transmission timing, each of said base stations being equipped with first delay means for giving a delay of a predetermined resolution to an input signal, comprising:

second delay means for giving a delay to an output signal of said first delay means with a higher resolution than said first delay means,

control means for computing a first delay amount which is a maximum value that does not exceed a predetermined delay amount and can be given by said predetermined resolution, instructing said first delay means said first delay amount, computing a second delay amount which is said first delay amount subtracted from said predetermined delay amount and instructing said second delay means said second delay amount,

transmission timing setting means for notifying said control means of said predetermined delay amount as a transmission timing, and

a transmission filter constituted by an oversampling filter being provided between said first delay means and said second delay means, wherein:

said resolution of said second delay means is equal to a sampling period of an output signal of said transmission filter.

6. – 8. (Cancelled)

9. (Previously Presented) A transmission circuit to be used in a mobile communications system which has a plurality of base stations for synthesizing and transmitting a plurality of input signals as a transmission signal and transmits said transmission signal from each of said

base stations with a matched transmission timing, said input signal being a spread signal obtained by spreading an information sequence based on a spread code, comprising:

first delay means for giving a delay of a predetermined resolution to each of said input signals,

synthesizing means for synthesizing a plurality of output signals output from said first delay means to acquire a synthesized signal,

second delay means for giving a delay of a high resolution to said synthesized signal to acquire said transmission signal,

control means for computing a first delay amount which is a maximum value that does not exceed a predetermined delay amount and can be given by a delay with said predetermined resolution, instructing said first delay means said first delay amount, computing a second delay amount which is said first delay amount subtracted from said predetermined delay amount and instructing said second delay means said second delay amount,

transmission timing setting means for notifying said control means of said predetermined delay amount as a transmission timing, and

a transmission filter constituted by an oversampling filter being provided between said first delay means and said synthesizing means, wherein:

said resolution of said second delay means is equal to a sampling period of an output signal of said transmission filter.

AFTER FINAL ENTER CLAIM

10. – 16. (Cancelled)

17. (Currently Amended) ~~The transmission circuit of claim 16,~~ A transmission circuit, comprising:

a plurality of first timing adjusting circuits, each first timing adjusting circuit of said plurality of first timing adjusting circuits configured to: (i) input a corresponding spread signal of a plurality of spread signals, (ii) delay the corresponding spread signal by a first delay stage quantity, and (iii) output a corresponding first timing output signal of a plurality of first timing output signals, said plurality of first timing adjusting circuits having a first resolution for specifying the first delay stage quantity;

a plurality of transmission filters, each transmission filter of the plurality of transmission filters configured to: (i) input a corresponding first timing output signal of the plurality of first timing output signals, (ii) oversample the corresponding first timing output signal in accordance with an oversampling period, and (iii) output a corresponding filter output signal of a plurality of filter output signals;

a plurality of second timing adjusting circuits, each second timing adjusting circuit of the plurality of second timing adjusting circuits configured to: (i) input a corresponding filter output signal of the plurality of filter output signals, (ii) delay the corresponding filter output signal by a second delay stage quantity, and (iii) output a corresponding second timing output signal of a plurality of second timing output signals, said plurality of second timing adjusting circuits having a second resolution for specifying the second delay stage quantity that is a higher resolution than said first resolution;

a synthesizer for synthesizing the plurality of second timing output signals to provide a transmission signal;

a plurality of spread code generating circuits, each spread code generating circuit of said plurality of spread code generating circuits configured to provide a corresponding spread code of a plurality of spread codes; and

a plurality of multipliers, each multiplier of said plurality of multipliers configured to multiply a corresponding information sequence of a plurality of information sequences by a corresponding spread code of the plurality of spread codes to provide a corresponding spread signal of the plurality of spread signals;

wherein a period of each spread~~ing~~ code of the plurality of spread~~ing~~ codes is the same; and

wherein each first timing adjusting circuit of the plurality of first timing adjusting circuits comprises a first-in-first-out (FIFO) memory with a size that is less than or equal to the period of a spread~~ing~~ code of the plurality of spread~~ing~~ codes.

AFTER FINAL

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18. (Currently Amended) The transmission circuit of claim 17,

wherein a sampling period of each spread~~ing~~ code of the plurality of spread~~ing~~ codes is the same; and

wherein each second timing adjusting circuit of the plurality of second timing adjusting circuits comprises a first-in-first-out (FIFO) memory with a size that is less than or equal to the sampling period of ~~a~~ the spread~~ing~~ code of the plurality of spread~~ing~~ codes divided by the oversampling period.

AFTER FINAL ENTER CLAIM

19. (Cancelled)

20. (Currently Amended) ~~The transmission circuit of claim 19,~~ A transmission circuit, comprising:

a plurality of first timing adjusting circuits, each first timing adjusting circuit of said plurality of first timing adjusting circuits configured to: (i) input a corresponding spread signal of a plurality of spread signals, (ii) delay the corresponding spread signal by a first delay stage quantity, and (iii) output a corresponding first timing output signal of a plurality of first timing output signals, said plurality of first timing adjusting circuits having a first resolution for specifying the first delay stage quantity;

a plurality of transmission filters, each transmission filter of the plurality of transmission filters configured to: (i) input a corresponding first timing output signal of the plurality of first timing output signals, (ii) oversample the corresponding first timing output signal in accordance with an oversampling period, and (iii) output a corresponding filter output signal of a plurality of filter output signals;

a plurality of second timing adjusting circuits, each second timing adjusting circuit of the plurality of second timing adjusting circuits configured to: (i) input a corresponding filter output signal of the plurality of filter output signals, (ii) delay the corresponding filter output signal by a second delay stage quantity, and (iii) output a corresponding second timing output signal of a plurality of second timing output signals, said plurality of second timing adjusting circuits having a second resolution for specifying the second delay stage quantity that is a higher resolution than said first resolution;

a synthesizer for synthesizing the plurality of second timing output signals to provide a transmission signal; and

a control section for inputting a desired delay amount and for determining the first delay stage quantity and the second delay stage quantity based on the desired delay amount;

wherein the desired delay amount is specified in terms of the second resolution;

wherein the control section is configured to calculate the first delay stage quantity as an integer by dividing the desired delay amount by a number that represents a number of samples at the second resolution that can be obtained for every one sample at the first resolution; and

wherein the control section is configured to calculate the second delay stage quantity as an integer that is ~~the~~ a remainder of the division when calculating the first delay stage quantity.

21. – 22. (Cancelled)